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Planar pixel detector module development for the HL-LHC ATLAS pixel system

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ABSTRACT

The ATLAS pixel detector for the HL-LHC requires the development of large area pixel modules that can withstand doses up to 10^{16} 1 MeV n_{eq} cm^{-2}. The area of the pixel detector system will be over 5 m^2 and as such low cost, large area modules are required. The development of a quad module based on 4 FE-I4 readout integrated chips (ROIC) will be discussed. The FE-I4 ROIC is a large area chip and the yield of the flip-chip process to form an assembly is discussed for single chip assemblies. The readout of the quad module for laboratory tests will be reported.

1. Introduction

The Large Hadron Collider (LHC) at CERN is the world's highest energy particle accelerator. At present it collides two proton beams each with a centre of mass energy of 7 TeV. One of the four large experiments on the LHC is the general purpose ATLAS [1] experiment. The tracking detector of the ATLAS experiment consists of, going from the vertex out to larger radius, a silicon pixel based system [2], a silicon microstrip based system (SCT) and finally a transition radiation tracker (TRT).

To realise the full physics potential of the LHC a series of luminosity upgrades are planned to the accelerator, resulting in the High-luminosity LHC (HL-LHC) [3,4]. The HL-LHC will have an order of magnitude increase in instantaneous and integrated luminosity over the LHC, from a few 100 fb^{-1} to 3000 fb^{-1} in 10–12 years of planned operation. To cope with the associated increase in event multiplicity and radiation damage the ATLAS experiment will also undergo a series of upgrades.

The increased occupancy, due to the high number of pile-up events per bunch crossing, necessitates a complete replacement of the ATLAS inner detector with a higher granularity system. The tracking system will be a full silicon system with, in the barrel region, 5 layers of silicon strip detectors extending from a radius of about 30 cm from the interaction point. Due to occupancy considerations, the strip length is divided into long (≈5 cm long, in the outer three layers) and short (≈2.5 cm long, for the inner two layers) strips. The four layer pixel detector system (with layers at radii of 39, 75, 160, and 250 mm) is located inside the strip system where occupancy and radiation damage become too large for strip detectors.

The expected maximum fluence will ultimately increase to a maximum level, at the innermost layer, of 2×10^{16} cm^{-2} 1 MeV equivalent neutrons (1 MeV n_{eq}) [5], consisting essentially of charged particles. The level falls to 10^{15} cm^{-2} 1 MeV n_{eq} at the outermost pixel layer. Such doses are unprecedented for silicon detectors and work on the design of detector systems that yield sufficient signal to noise performance are under way. The leading sensor technology under investigation, presented here and elsewhere in this proceedings [6], is the planar silicon sensor with a p-type bulk and n-type segmented implants. The sensor technology for the inner most radius is still more open for investigation with 3D silicon and diamond sensors, as well as planar silicon, also being investigated.

Due to the large size of the pixel system, large area pixel modules are being investigated. The development work uses the FE-I4 [7] chip that has been developed for the ATLAS inner B-layer upgrade (IBL) [8]. The FE-I4 ROIC is produced in 130 nm CMOS technology, which allows for a smaller pixel size, increased in-pixel processing power and reduced power dissipation compared to the present ATLAS pixel ROIC the FE-I3 [9]. For zero pixel occupancy the FE-I4 draws 675 mW, (195 mW cm^{-2}), compared to the FE-I3 which draws 220 mW (380 mW cm^{-2}). The individual pixel size is reduced from the present 50×400 μm^2 to 50×250 μm^2 to cope with the increase in hit occupancy. The 50 μm dimension has been kept to allow the flip-chip processing to take place.

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The FE-I4 is the largest ROIC produced for particle physics applications and is nearly six times larger in area that the present FE-I3 ROIC (3.36 cm^2 compared to 0.58 cm^2 of active area). The proposed pixel system will use modules that consist of 2×2 FE-I4 ROICs, (known as a quad module). The pixel modules aim to have a high active area (≈90%), which is achieved through the use of a large area ROIC with minimised dead space due to periphery pixel chip logic and control circuits. To reduce mass the ROIC will be thinned to 150 μm or less. The sensor will also be 150 μm thick, which has the additional benefit of reduced sensor power load, as well as mass reduction. The data from the 4 FE-I4 ROICs on a module will be multiplexed together to reduce the material due to the signal lines. The system will use serial powering to reduce the amount of material in the services; via less material in the power cable and in the cooling system.

The paper presents work on the design of silicon sensors produced at Micron Semiconductor Ltd,[1] the yield of thin ROICs flip-chip bonded at VTT[2] to these sensors, and the first results from a quad module.

2. Sensors

Two sensor wafer designs that are compatible with the FE-I4 ROIC have been produced at Micron Semiconductor Ltd. They have been fabricated on 6 in. 10 kΩ cm p-type float zone silicon wafers. The segmented side is a heavily doped n-type implant with a p-spray isolation between them. Wafers of 300 μm and 150 μm in thickness have been produced. Results only from the 300 μm devices are shown here. These devices show a full depletion voltage, before irradiation, of 70 V, as expected from their resistivity.

The first of the two wafers, known as CERN Pixel II, has pixel sensor arrays compatible to the FE-I4 readout chip. There are 14 single and 5 two chip FE-I4 sensor designs. The two chip design has a guard structure around the pixel array that matches two FE-I4 chips. The inter-chip region is filled with active silicon. This is achieved with the use of an implant on the last column of one chip and the first of the next of 450 μm in length rather than 250 μm. The single sensors include three different guard ring structures. Two designs have 8 guard rings that are 390 μm wide in total, while the third set has only 4 guard rings with a total width of only 200 μm. This design is known as the slim edge sensor. Sensors with reduced dead space at the edge are attractive for building particle physics experiments as it allows the close packing of the modules on a stave. This removes the requirement to shingle modules on two surfaces of a stave structure, resulting in a lower mass, easier to build system. Such an assembly approach has been required by the ATLAS IBL due to space limitations. For the full HL-LHC upgrade a similar approach is also desired.

The second wafer, known as CERN Pixel IV, has 5 quad sensors and 8 single chip FE-I4 designs. One of the quad sensors includes a slim edge design. The quads have been designed with the inter-chip region filled with active silicon. This is achieved with the use of an implant on the last column of one chip and the first of the next of 450 μm in length rather than 250 μm, as with the two chip sensor design. The separation between the two chips in the row direction is either 850 μm or 450 μm. The area remains active with the use of eight or four extra pixel implants per ROIC. These are attached one each to the outer four pixels, and as such, are connected to the ROIC. When these are hit there is a two pixel ambiguity which needs to be resolved with the use of the tracking system. The design of top metal layer of the pixel sensor is shown in Fig. 1 for the area where the four FE-I4 ROICs are bonded for the design with four extra pixel implants between each ROIC.

Two of the single chip sensors on this wafer have an implant that is 25×500 μm^2 in size rather than the 50×500 μm^2 of the read-out cell. This is achieved with the pixel bump pads being in the same position as the standard sensor, and therefore maintains compatibility with the FE-I4 ROIC. Such a design will enable increased r–Φ resolution in the detector for the same pixel area, but with a reduced resolution in the z-direction.

The single chip sensors current-voltage characteristics showed a current of approximately 10 nA at a reverse bias voltage of 90 V, which is above full depletion. This corresponds to a current density of better than 3 nA cm^{-2} measured at a temperature of 20 °C. The breakdown voltage of the device was design dependent. The best devices were able to hold 1000 V, while the more typical value was 400 V. The slim edge devices typically showed a dramatic increase in current at 150 V, which is to be expected in a non-irradiated device as with bias the depletion region extends laterally to the cut edge.

Building on the success of the two CERN Pixel wafer designs a new sensor wafer is under development. One of its aims is to investigate sensors that are compatible with the FE-I4 ROIC that have alternative implant structures, for example square pixels. Such a pixel structure might lead to benefits in the forward, high pseudo-rapidity region of the detector system, covered by the pixel disk system.

3. Single chip assemblies

Four sensor wafers, two of each design, and three FE-I4 ROIC wafers were shipped to VTT for under-bump metal deposition (UBM), lead-tin solder ball deposition and flip-chip assembly. Both the sensor and ROIC wafers had the UBM deposited upon them. Only the ROIC had the PbSn electroplated and reflowed to form solder bumps. After solder bump deposition one of the two ROIC wafers was back thinned to a thickness of 200 μm. This represented the first stage at making assemblies with thin ROICs required for the ATLAS HL-LHC pixel system. The ROIC wafers were diced and the bumps visually inspected for missing or shorted bumps. The yield of the bump deposition and re-flow process was high with only 12% of the ROICs being rejected due to poor bump yield; defined as more than 25 faulty bumps in the matrix of 26880 bumps, corresponding to 0.1%.

The ROICs were flip-chipped to the sensors with an FC-150 SET machine at VTT. A weak tack bond was made on the machine. The assemblies were then transferred to a re-flow oven, with a reducing atmosphere, to reflow the solder bumps at 260 °C. The sensor and ROIC were held on SiC vacuum jigs on the FC-150 machine. However, in the re-flow oven they are not held flat under vacuum and could therefore bow.

Fifteen single chip assemblies have been produced all with ROICs from the 200 μm thick wafer. Of these, 5 assemblies have been mounted onto test cards and tested in the laboratory and at test-beams. The other 10 devices have not been mounted and will be sent for irradiation to prove the radiation hardness of the assemblies.

The sensor wafers were all probed after fabrication while on the wafer, after UBM deposition and wafer dicing and after assembly into a module. The current-voltage characteristics of the sensors did not change relative to the initial measurements, except that a few showed a slightly improved high voltage characteristic, as illustrated in Fig. 2.

The tested devices have been characterised with the use of the USBPix test system [10] in the laboratory at a temperature of 20 °C and at test-beam (not reported here). The goal of the laboratory characterisation was to prove the yield of the flip-chip process and the noise performance of the modules. The initial characterisation stage required the tuning of the DACs that control the in-pixel

[1] Micron Semiconductor Ltd. www.micronsemiconductor.co.uk.
[2] VTT Technical Research Centre of Finland, http://www.vtt.fi.

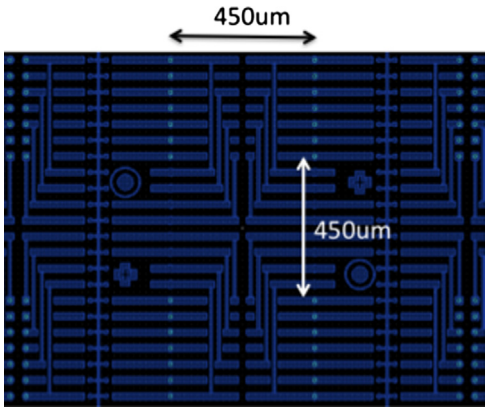

Fig. 1. Detail of quad pixel sensor design showing the top metal layer for the region where four FE-I4 chips are bonded.

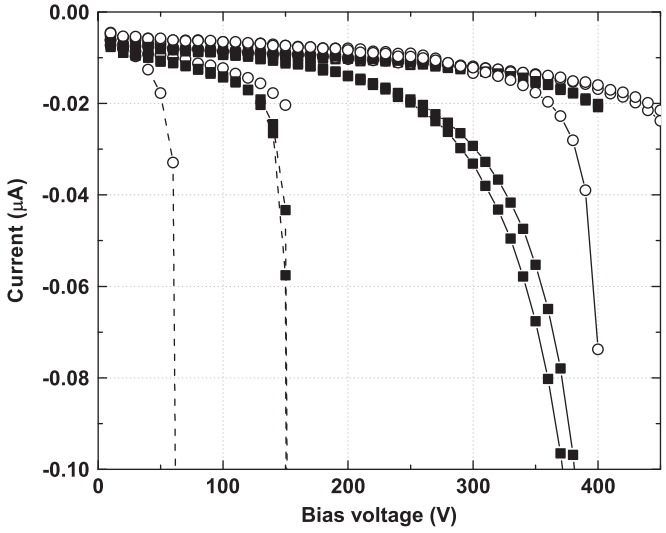

Fig. 2. The current–voltage characteristics of 6 reversed bias Micron FE-I4 single chip sensors measured on wafer (closed squares) and after assembly into modules (open circles). The two slim edge sensors are distinguished by dashed lines. Measurement temperature of 20 °C.

amplifier feedback current and the in-pixel discriminator threshold value per pixel. The sensor was biased to 100 V during the tuning of the assemblies. The tuning of the modules was performed with a target threshold value of 3200 electrons and a time over threshold value of 8 counts for an input charge of 20,000 electrons. The ToT is measured in units of 25 ns duration, which is defined by an externally supplied clock running at 40 MHz, as this corresponds to the bunch crossing rate of the LHC. The modules were then tuned down to a threshold value of 1600 electrons, which is the target threshold for the IBL.

The assemblies, after tuning, demonstrated a low threshold dispersion across the matrix (23 in 3200 electrons) with a noise, derived from the *s*-curves, of 130 ± 6.7 electrons.

After tuning the devices were characterised. The first scans performed a digital and analogue test of each pixel element. This allowed dead pixels to be counted and masked. Four of the assemblies had no dead pixels, with the fifth having only 35. It is not known if these were present in the ROIC before processing. The next set of scans removed pixels that were "stuck-on" 01wand finally pixels with a high noise occupancy were removed. On average for the 5 assemblies tested there were only 3 pixels in the matrix that showed high noise occupancy and none that were "stuck-on". Once these pixels were removed from the matrix the bump quality was investigated.

The cross talk between one pixel and its neighbour was measured to understand the number of merged bumps. The detector was again biased to 100 V to over deplete the device. A very large charge, significantly above the threshold value, was injected in pixels $n-1$ and $n+1$ of a given column, while pixel n was readout. It has been shown that for an un-bonded FE-I4 it is not possible to cause cross-talk with the maximum possible injected charge. It is also known that for a fully depleted detector attached to the ROIC no cross-talk should be visible for a threshold of 3200 electrons. Therefore if cross-talk is observed the pixel front-ends must be electrically connected via a merged bump bond. The average number of merged bonds in the 5 assemblies was 2, which is a high yield.

The final set of measurements characterised the single chip assemblies for un-bonded pixel channels. There are two main causes of an un-bonded pixel; poor or missing bump on the ROIC or bow in the assembly during reflow or initial tack bonding. The visual inspection of the ROICs before the flip-chip process rejected any ROIC that had more than 25 defective bumps. Therefore, if any significant number of un-bonded pixels were measured then the flip-chip and reflow process would be at fault.

Three methods were used to investigate the number of un-bonded pixels, namely: pixel noise, pixel cross-talk and response to 60 KeV gamma rays from an Am-241 source. The noise of an un-bonded FE-I4 is between 120 and 130 electrons. When it is bonded to a fully depleted planar silicon detector the noise is between 130 and 150 electrons. Therefore it is not possible to distinguish un-bonded pixels with this method for a biased detector. However, when the detector is not biased the capacitive load on the front-end due to the undepleted detector is significant and the noise increases to approximately 500 electrons. A histogram of noise at the target threshold was made for each assembly without detector bias. Two distinct peaks were visible, one centered on 120 electrons and other centered on 500 electrons. The low noise pixels, (un-bonded pixels), were all distributed at the edge of the matrix, with the corners being most effected. An example of the results from the noise measurement is shown in Fig. 3. The number of un-bonded pixels measured by this method on this assembly is 628, which corresponds to 6.5% of the pixels in the matrix. The number of un-bonded channels varied significantly between assemblies, as summarised below.

The second method takes advantage of the fact that an unbiased detector has strong capacitive coupling between each pixel element. Therefore a measurement of cross-talk will inject charge in neighbouring channels if they are both bonded to the pixel electronics. A cross-talk scan was performed on each assembly for 0 V sensor bias and the channels without cross-talk recorded and compared to the un-bonded pixel numbers from the noise measurement. The number of un-bonded channels from this measurement was on average 5% higher than for the noise measurements, but showed the same spatial distribution over the matrix.

The assembly with the $25 \times 500\ \mu m^2$ implants never showed cross-talk without detector bias, while the noise measurements indicated a significant fraction on bonded pixels. The reason for this was due to the fact that the sensor implants that had charge injected into them were shielded from each other due to the altered implant structure. The cross-talk measurement was therefore not appropriate for this detector design without a change in the charge injection map.

The first two measurements are attractive methods to measure the bump bond yield as they are purely electrical and can be performed on a probe station before the assembly is made into a

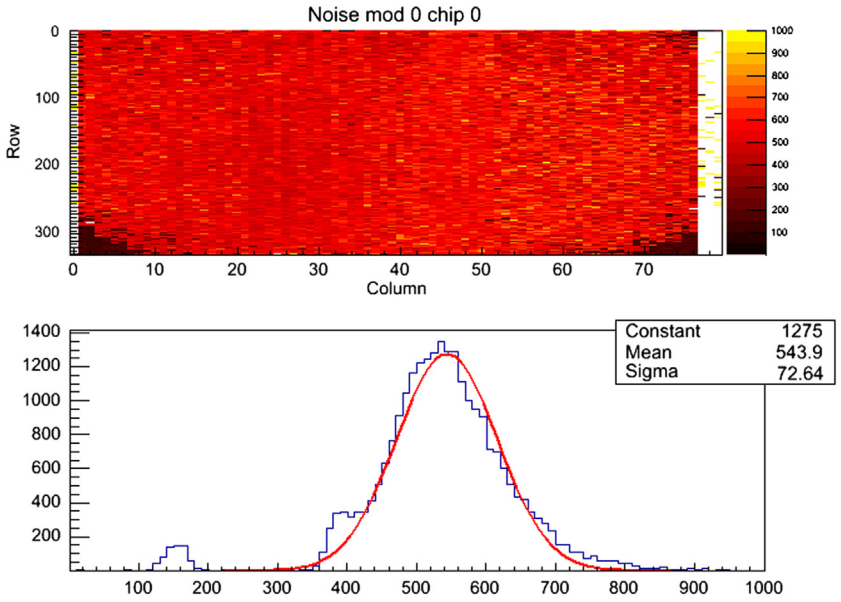

Fig. 3. Top plot shows the map of the noise measured over a pixel assembly with no sensor bias, measured in electrons, shown on the right hand scale. The associated histogram of the noise data is given in the lower plot. The low noise peak is due to un-bonded pixel channels distributed at the edges and corners of the pixel matrix. This assembly has 628 un-bonded pixels, or 6.5% of the pixels in the matrix. Measurement temperature of 20 °C.

module with the addition of a flex PCB. This will enable the screening of pixel chips during the module production phase and allow assembly re-work before the addition of the flex PCB.

Finally the bump bond yield was measured with the 60 KeV gammas from an Am-241. Care was taken to shield the assembly from the 5.5 MeV alpha particles also emitted from the source as this disrupts the response of the matrix. The source, of diameter of 5 mm, was placed 20 cm from the sensor to allow complete illumination of the device. The sensor was biased to 100 V. The readout system was triggered using the HitOr output from the pixel matrix itself (that is, the system was self triggered). This is only possible for devices where all "stuck-on" or high noise occupancy pixels are masked, otherwise these will saturate the HitOr bus. Source measurements were made for more than 3 million events per assembly, which gave a maximum pixel count of 200 in the area directly under the source and 50 counts at the edge of the pixel assembly. Again the assemblies showed the same pattern of un-bonded pixels at the corners and along the edges of the assembly. The number of un-bonded channels was again similar to the number measured with the purely electrical measurements, which adds confidence in these methods being applied as a bump bond quality control.

The best assembly had 3% of the channels un-bonded, while the worse assembly showed 66% un-bonded channels. The reason for the low bond yield is believed to be due to the bow in the ROIC during the re-flow process. As mentioned above, the re-flow process takes place at elevated temperature (260 °C) while the ROIC is not pulled flat on a vacuum jig. The ROIC has a thick stack of dielectric on the top CMOS side (between 15 and 20 μm), which has a built in stress. The built-in stress and the stress resulting from the difference in the coefficient of thermal expansion, (CTE), between the dielectric and silicon results in a bow in the thin ROIC. The sensor wafer also has a dielectric layer on the top side, which faces the ROIC, and undergoes a bow due to CTE mismatch. The sensor therefore bows away from the ROIC. The bow is sufficient to pull the tack bonded solder bonds apart causing bond failure at the edges of the assembly.

Solutions to over come this low bond yield are being studied and include temporary support wafers and the deposition of balancing dielectric layers on the ROIC and sensor wafers.

4. Quad modules

Ten 300 μm thick CERN Pixel IV wafers have been produced and characterised electrically on wafer. The sensors again fully deplete at 70 V, as expected from the wafer resistivity. The leakage current, measured at 90 V and a temperature of 20 °C, was 3 nA cm^{-2} as with the single devices. The maximum safe bias that can be applied to the sensors is typically 500 V, compared to 1000 V for the singles. The yield is also lower with only 70% of the devices holding 100 V. The reason for the lower yield is due to the larger perimeter of the device and therefore increased risk of defects appearing in this region. However, the good devices perform as well as the single devices from the point of view of current density just above full depletion voltage. The high voltage characteristics are expected to improve after an irradiation dose, as is generally observed in silicon detectors.

Two CERN Pixel IV wafers were sent to VTT for UBM deposition and flip-chip assembly into 5 quad assemblies. The first quad was made with 200 μm thick ROICs but, after the measurements of the low bump yield, the remaining were assembled with full thickness (750 μm) ROICs. The current-voltage characteristics of the sensor in the assembly was unchanged from the pre-assembled devices.

The quad assemblies have allowed the first quad module to be fabricated. A simple single layer kapton flex, supplied by the Bonn group, was glued to the sensor and used to route signal and power from the USBPix system to the FE-I4 chips. The interconnect between bus lines and each chip, normally performed in a second metal layer, was accomplished with wire bonds. The USBPix system is unable to read data from 4 FE-I4s and therefore a switch was used to read data from a single chip at a time. To achieve this, the quad module was mounted in a PCB frame which routes the 4 sets of LVDS output data lines to a set of switches, and on to a KEL connector, for connection to the USBPix system. The PCB also regulated locally the low voltage supply for the 4 FE-I4s, from a 3 V bench power supply.

After module assembly the sensor current-voltage characteristics remain unchanged. The module was successfully configured and data received from the ROICs. The module has been tuned to a target threshold of 3200 electrons with a ToT value of 8 for an input charge of 20,000 electrons. Detailed characterisation of the module

is presently taking place. The next phase of the development is to develop an FPGA based multiplex board to allow all four FE-I4 chips to pass data at the same time to an external DAQ system. In hand with this, a two layer flex hybrid is being designed.

5. Conclusions

The development of a sensor technology for the ATLAS pixel system upgrade for the HL-LHC is progressing well. Single chip and quad module sensors and assemblies have been made. The current characteristics of the sensors are good. A slim edge device has been fabricated and is able to hold a bias voltage 100% higher than the full depletion voltage of the sensor before irradiation. Pixel detectors compatible with the FE-I4 ROIC but with different implant geometries have been produced and have been shown to work in laboratory tests.

Characterisation methods for the FE-I4 assemblies have been developed. The assemblies produced to date at VTT have shown an unacceptably low bump bond yield. The cause of this is believed to be bow in the ROIC and the sensor during the re-flow process. Investigation into a method to over come this problem is taking place.

The first quad FE-I4 modules have been fabricated and shown to work. At present data is only read from one chip at the time, while all chips are clocked and configured. Future development of a multiplex board will allow the data from all four chips to be read out is underway.

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